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(71) Applicant *(for all designated States except US)*: **LENSLET LTD.** [IL/IL]; 12 Hahilazon Street, 52522 Ramat-Gan (IL).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **LEVY, Ron** [IL/IL]; 10/10 Hanita Street, 44405 Kfar-Saba (IL). **ASAF, Yosefa** [IL/IL]; 15/4 Levona Street, 71700 Modin (IL). **GOREN, Avner** [IL/IL]; 4 Sitvanit Street, Givat Tal, 48581 Rosh Haayin (IL). **GROSS, Yoram** [IL/IL]; 14/3 Shapira Shmuel Street, 75284 Rishon Lezion (IL).

(74) Agents: **FENSTER, Paul** et al.; Fenster & Company Patent Attorneys, LTD., P.O. Box 10256, 49002 Petach Tikva (IL).

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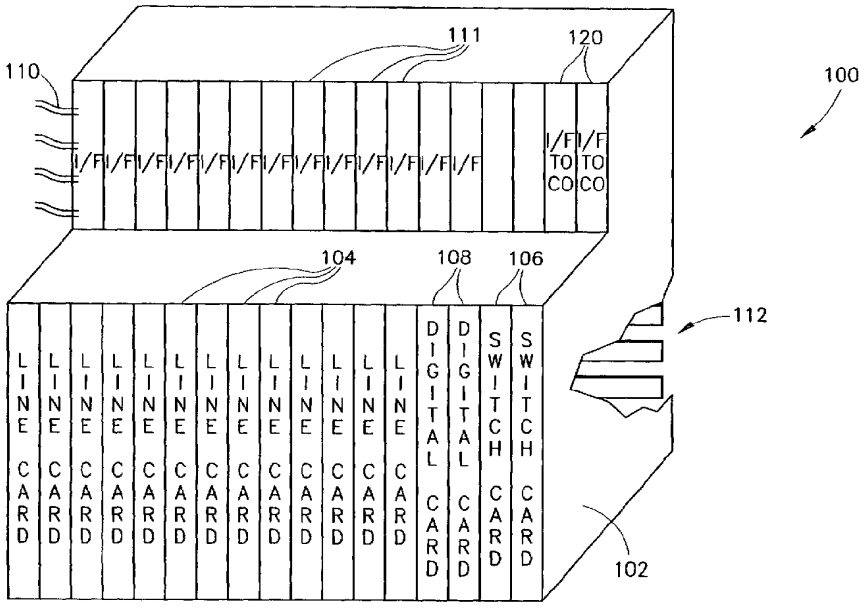
(54) Title: ADSL ACCESS MULTIPLEXER



(57) Abstract: A method of handling an ADSL connection by an access multiplexer (100), comprising: receiving a data segment to be transmitted by the access multiplexer (100); performing digital processing of the data segment by a digital card (108); locally transferring the digitally processed data segment to a line card (104) separate from the digital card (108); performing at least analog processing of the data segment by the line card (104); and transmitting the analog processed data segment on the ADSL connection.

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ADSL ACCESS MULTIPLEXER

FIELD OF THE INVENTION

The invention relates to transmitting information using ADSL systems and particularly to ADSL multiple access multiplexers.

BACKGROUND OF THE INVENTION

The asynchronous digital subscriber line (ADSL) protocol is used to transfer data at high speeds on standard copper wire telephone lines. The ADSL protocol is carried out by a client ADSL modem at a user's premises and a respective access ADSL modem at a nearby central office (CO). Generally, the access ADSL modems are included in a multiple access multiplexer rack which includes a plurality of line cards, each of which cards handles a predetermined number of ADSL connections. The rack also includes one or more switch cards which connect to a communication network. The ADSL tasks performed by the ADSL modems generally comprise analog tasks (e.g., echo cancellation, automatic gain control, analog to digital and digital to analog conversions) and digital tasks (e.g., Fourier transforms, Quadrature Amplitude Modification ("QAM") modulation, forward error correction, interleaving). In addition, the rack may also perform other, non-ADSL, tasks, such as billing tasks. The non-ADSL tasks are generally performed by a separate management card included in the rack or by apparatus external to the rack.

In order to reduce the cost of the ADSL service, it is desired to maximize the number of connections handled by each access multiplexer rack. The size and shape of the ADSL racks, however, are predefined by an industry standard. Each line card generally includes, for each ADSL connection it handles, an analog unit which performs the analog tasks of the connection. In addition, each line card includes a digital unit which performs digital tasks for all the ADSL connections it handles. Currently, a line card can carry about 8-16 analog units together with the digital unit. Attempts are being made to reduce the sizes of the analog and digital units so that 32 analog units will fit on a single card.

Due to the nature of ADSL technology, communication over the copper lines is limited to a maximal distance of about 3-6 km. Therefore, the ADSL access rack must sit within 3-6 kilometers from the client ADSL modems. Generally, a rack is placed in each neighborhood even if the neighborhood includes only a few ADSL users. The placement of racks which are not used at their capacity is costly.

EP 0 831 624, the disclosure of which is incorporated herein by reference describes an ADSL data analysis system with various features.

SUMMARY OF THE INVENTION

An aspect of some embodiments of the present invention relates to an ADSL access multiplexer (DSLAM) which includes a plurality of separate cards that together perform the handling tasks of a single ADSL connection. In some embodiments of the invention, an ADSL access multiplexer comprises separate cards for analog and digital tasks. One or more analog cards optionally perform the analog tasks for all the connections handled by the DSLAM and one or more digital cards perform the digital tasks of the connections. By dividing the handling tasks between a plurality of cards, it is possible to use processing units which can handle more ADSL connections than for which it is possible to position analog handling units on a single card. Alternatively to providing separate cards, separate units are provided on a same card. For example, one analog unit may service multiple digital units or vice versa. Alternatively, several analog and several digital units may be provided, for example on a same card or in a same rack (or other local unit arrangement), with the association of analog units with digital units being performed as needed.

An aspect of some embodiments of the present invention relates to an ADSL access multiplexer which performs the ADSL tasks of a single connection by a plurality of separate units located at separate locations. Optionally, the digital tasks are performed at a separate location from the analog tasks, but in a same locale. In an exemplary embodiment of the invention, the units are locally positioned, for example in a same rack or box, in nearby racks, or in a same building. Alternatively, the separate locations may be distanced by tens, hundreds, thousands or evens tens of thousands of meters, or more. Thus, it is possible to locate only a small percentage of the apparatus required for handling the ADSL connections near the user's premises while the remaining apparatus is located at a central location.

There is thus provided in accordance with an exemplary embodiment of the invention, a method of handling an ADSL connection by an access multiplexer, comprising:

receiving a data segment to be transmitted by the access multiplexer;

performing digital processing of the data segment by a digital card;

locally transferring the digitally processed data segment to a line card separate from the digital card;

performing at least analog processing of the data segment by the line card; and

transmitting the analog processed data segment on the ADSL connection. Optionally, performing the digital processing by the digital card comprises performing a Fourier transform. Alternatively or additionally, performing the digital processing by the digital card comprises performing substantially all the digital processing tasks required for transmission of ADSL data. Alternatively, performing the digital processing by the digital card comprises performing fewer than all the digital processing tasks required for transmission of ADSL data.

In an exemplary embodiment of the invention, the line card performs substantially only analog tasks. Alternatively or additionally, the line card performs at least one digital ADSL task.

In an exemplary embodiment of the invention, transferring the digitally processed data to the line card comprises transferring over a backplane bus of a rack hosting both the line card and the digital card. Alternatively, transferring the digitally processed data to the line card comprises transferring to a different rack in a same locale.

In an exemplary embodiment of the invention, transferring the digitally processed data to the line card comprises transferring through an optical fiber.

There is also provided in accordance with an exemplary embodiment of the invention, a method of transmitting data on a plurality of ADSL connections, by an access multiplexer, comprising:

receiving a plurality of data segments, to be transmitted on a plurality of different ADSL connections, by the access multiplexer;

performing digital processing of the data segments by a digital card;

locally transferring at least one of the digitally processed data segments to a first line card and at least one of the digitally processed data segments to a second line card, separate from the first line card;

performing, by the first and second line cards, at least analog processing of the data segments transferred to the line cards; and

transmitting the analog processed data segment on their respective ADSL connections. Optionally, the first and second line cards are not positioned in a common rack. Alternatively, the first and second line cards are positioned in a common rack.

There is also provide din accordance with an exemplary embodiment of the invention, a method of handling an ADSL connection by an access multiplexer, comprising:

receiving an analog data segment from the ADSL connection, by a line card;

performing at least analog processing of the data segment by the line card;

locally transferring the analog processed data segment to a digital card separate from the analog card; and

performing at least one ADSL digital processing task of the data segment by the digital card. Optionally, performing the digital processing by the digital card comprises performing substantially all the digital processing tasks required for reception of ADSL data. Alternatively, performing the digital processing by the digital card comprises performing fewer than all the digital processing tasks required for reception of ADSL data.

There is also provided in accordance with an exemplary embodiment of the invention, a DSL access multiplexer, comprising:

at least one line card including one or more analog units adapted to transmit signals on one or more respective ADSL connections;

a digital processing card adapted to perform at least one digital ADSL handling task on signals to be transmitted; and

a local communication link adapted to transfer signals processed by the digital processing card to one of the at least one line cards. Optionally, the at least one line card includes substantially only analog units. Alternatively or additionally, the at least one digital processing card includes a Fourier transform unit. Alternatively or additionally, the communication link comprises a backplane of a rack adapted to receive the at least one line card and the digital processing card. Alternatively or additionally, the communication link comprises an optical fiber.

There is also provided in accordance with an exemplary embodiment of the invention, a DSL access multiplexer, comprising:

at least 64 analog units adapted to transmit signals on one or more respective ADSL connections; and

a single digital processing unit adapted to perform at least one digital ADSL handling task on signals to be transmitted by all the at least 64 analog units. Optionally, the at least 64 analog units are included in a plurality of line cards.

BRIEF DESCRIPTION OF FIGURES

Non-limiting examples of embodiments of the present invention are described below with reference to figures attached hereto. In the figures, identical structures, elements or parts that appear in more than one figure are generally labeled with the same numeral in all the

figures in which they appear. Dimensions of components and features shown in the figures are generally chosen for convenience and clarity of presentation and are not necessarily shown to scale. The figures are listed below.

Fig. 1 schematically shows an ADSL access multiplexer (DSLAM), in accordance with an embodiment of the present invention;

Fig. 2 is a schematic block diagram of an analog line card of a DSLAM, in accordance with an embodiment of the present invention;

Fig. 3 is a schematic block diagram of a digital processing card of a DSLAM, in accordance with an embodiment of the present invention;

Fig. 4 is a schematic block diagram of the hardware elements of the digital processing card of Fig. 3, in accordance with an embodiment of the present invention; and

Fig. 5 is a schematic illustration of a distributed ADSL access multiplexer, in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Fig. 1 schematically shows an ADSL access multiplexer (DSLAM) 100, in accordance with an embodiment of the present invention. DSLAM 100 comprises a rack 102 in which a plurality of analog line-cards 104 which perform the analog tasks of DSLAM 100, are positioned. In some embodiments of the invention, each analog line card 104 has a respective line interface (I/F) 111 to which the line card 104 is connected within rack 102. Line interface 111 physically connects the respective line card 104 to one or more copper wire pairs 110 (shown for clarity with only one of line interfaces 111), on to which the line card 104 transmits signals and from which the line card 104 receives signals. Optionally, line interfaces 111 include splitters (not shown) which connect to both telephone lines and ADSL lines. Alternatively or additionally, some or all of wire pairs 110 lead to an external splitter (not shown). The use of an external splitter reduces the number of wires which need to connect to line interfaces 111. Further alternatively or additionally, line cards 104 connect directly to copper wire pairs 110.

Line card 104 may be connected permanently to a predetermined set of copper wire pairs 110, or may be connected dynamically to the copper wire pairs, for example through a switching system (not shown). In addition, DSLAM 100 includes a switch card 106, which connects DSLAM 100 to a communication network, for example through an Internet service provider (ISP). Optionally, switch card 106 has a respective interface 120 to which links

leading to the communication network are connected. As is known in the art, multiplexer 100 may include two or more cards 106 for redundancy (backup) and/or enhancement purposes.

Optionally, switch card 106 comprises, for each ADSL connection, transmission and reception buffers (not shown). The transmission buffers accumulate data to be transmitted while waiting for the turn of the connection to be processed by DSLAM 100. Similarly, the reception buffers accumulate data received by DSLAM 100 until the data is passed to the communication network. In some embodiments of the invention, switch card 106 may be used both in DSLAMs known in the art and with DSLAM 100, with substantially no changes. Alternatively, switch card 106 is adapted to be used in accordance with the present invention and cannot be used (without adaptation) in prior art DSLAMs.

One or more digital processing cards 108 perform the digital processing tasks of substantially all the ADSL connections handled by DSLAM 100. In some embodiments of the invention, digital processing card 108 performs the digital tasks for at least 64, 128, or even 256 ADSL connections. In an exemplary embodiment of the invention, DSLAM 100 includes two digital processing cards 108 of which one is for redundancy purposes. Optionally, a backplane bus 112 is used to transmit data between line cards 104, switch cards 106 and digital processing cards 108. Backplane bus 112 optionally comprises a high capacity bus, e.g., a giga-Ethernet bus or an optical fiber bus, suitable to carry the data transmitted between cards 108, 106 and 104. In some embodiments of the invention, backplane bus 112 includes a plurality of separate physical portions, so as to increase the capacity of the bus.

In some embodiments of the invention, the times of usage of backplane bus 112 by each of cards 108, 106 and 104 are set synchronously, such that collisions are not possible between data from different cards. Alternatively or additionally, backplane bus 112 includes a plurality of separate segments on which data from different sources are transmitted. The separate segments may include, for example, physically separate segments, different time zones, different frequency zones and/or different code zones. Optionally, bus 112 includes segments for transmission from switch card 106 to digital card 108, from digital card 108 to line cards 104, from line cards 104 to digital card 108 and from digital card 108 to switch card 106.

Fig. 2 is a schematic block diagram of an analog line card 104, in accordance with an embodiment of the present invention. Analog line card 104 optionally comprises a power supply 280, a bus interface 240 and a plurality of analog paths (AP) 209, which each handles

the analog tasks of an ADSL connection. Alternatively, rack 102 includes a power supply common to a plurality of cards 104, 106 and/or 108. Line card 104 optionally comprises between about 70-100 analog paths 209 (relative to 16-32 paths in cards of the prior art), although with the advance of circuit technology more analog paths 209 may fit on a single card 104. The additional analog paths 209 which fit on to card 104 are due to the fact that card 104 does not include digital processing units which generally occupy between 50-70% of the area of the card, in prior art line cards. Furthermore, separation zones required between digital and analog areas of the line card are not required, as line card 104 includes only analog zones.

In some embodiments of the invention, bus interface 240 receives signals for transmission from backplane bus 112 and passes the signals to the respective analog path 209 to which they are directed. In addition, bus interface 240 receives signals from the analog paths 209 and passes them to digital processing card 108. Alternatively, line card 104 includes separate bus interfaces for transmission and reception and/or for different groups of analog paths 209.

Optionally, bus interface 240 comprises a packet based interface, such as an ATM TC layer and/or an Ethernet interface. In some embodiments of the invention, bus interface 240 comprises a compression unit which compresses and/or decompresses the signals transmitted on backplane bus 112. Alternatively, signals are transmitted on backplane bus 112 uncompressed. Optionally, bus interface 240 comprises a flow control and/or error correction unit which verifies that the signals transmitted on backplane bus 112 are received correctly. Alternatively or additionally, backplane bus 112 is a highly reliable bus with a very low error rate.

Analog paths 209 comprise any type of analog path known in the art, for example as described in the ITU G992 recommendation, the disclosure of which is incorporated herein by reference. Generally, analog path 209 performs echo cancellation, automatic gain control and line protection. In addition, analog path 209 converts the analog signals received on wire pairs 210 to digital signals transmitted on backplane bus 112 and the digital signals received from bus 112 to analog signals to be transmitted on wire pairs 110.

Fig. 3 is a functional schematic block diagram of a digital processing card 108, in accordance with an embodiment of the present invention. Digital processing card 108 comprises an input bus interface 302 which receives signals to be transmitted on copper wire pairs 110 from switch cards 106 (Fig. 1), over backplane bus 112. A transmission path 300

processes the signals received by input bus interface 302, in accordance with the ADSL protocol. The processed signals are then forwarded to a respective analog line card 104 through an output bus interface 332.

In some embodiments of the invention, line card 108 comprises a second input bus interface 352 that receives data signals from line cards 104. Optionally, the signals received by bus interface 352 are processed by a reception path 350. The processed signals from reception path 350 are passed to an output bus interface 354 which forwards the signals to switch card 106 over backplane bus 112. In addition, digital processing card 108 optionally comprises a power supply (not shown).

In some embodiments of the invention, transmission path 300 comprises a CRC unit 306, a scrambler 308, a forward error correction unit (FEC) 310, an interleaver 312, a framer 314, a tone ordering unit 316, a mapper 318, an inverse Fourier unit 326, a shifter 328 and an IIR filter 330, which perform the tasks defined by the ADSL standard known in the art. Optionally, interleaver 312 comprises an interleaver engine 322 and an interleaver memory 324. In some embodiments of the invention, mapper 318 comprises a QAM mapper. Alternatively or additionally, mapper 318 comprises any other type of mapper, such as a trellis coding mapper. Optionally, mapper 318 comprises a mapper engine 317 and a mapper memory 319.

In some embodiments of the invention, reception path 350 comprises an IIR filter 353, a time equalizer (TEQ) 356, a Fourier transform unit 358, a frequency equalizer (FEQ) 359, a mapper 360, a tone order engine 362, an interleaver 364, a FEC decoder 370 and a CRC descrambler 372, which perform the tasks defined by the ADSL standard known in the art. In some embodiments of the invention, mapper 360 and interleaver 364 comprise operational engines (390 and 392, respectively) and memory units (394 and 396 respectively).

The units of transmission path 300 and reception path 350 perform the same tasks as known in the art. Optionally, the units of transmission path 300 and reception path 350 also comprise standard designs known in the art. It is noted, however, that in some embodiments of the invention, these units operate at faster clock rates than in the prior art as they may service more connections. In accordance with some embodiments of the present invention, instead of each line card 104 including a digital unit which operates at a clock rate lower than its capability, digital card 108 includes fewer digital units (e.g., fewer than the number of line cards 104 it services) which operate faster than units of the art, optionally close to their

maximal rate capability. If necessary, some or all of the units are duplicated in order to provide handling at a sufficient rate.

In some embodiments of the invention, data from the output buffers of switch card 106 is fed at a predetermined rate (defined by the ADSL protocol) through digital processing card 108 to line cards 104. Optionally, the data segments are fed from switch card 106 responsive to data requests generated by digital card 108. The data requests optionally state the connection for which data is requested and the amount of data required according to the service agreement of the connection. Alternatively, the data is fed by switch card 106 without receiving data requests from digital card 108. This alternative reduces the amount of signals transmitted on backplane bus 112, but mat require additional memory and/or logic units. Transmission path 300 of digital processing card 108 optionally operates synchronously at the predetermined rate, such that at each cycle of the predetermined rate, a first data segment is received by input interface 302 and a second, processed, data segment is forwarded by output bus interface 332. In some embodiments of the invention, the tasks of transmission path 300 are performed by a plurality of units, each of which units performs its tasks in one or more clock cycles, according to a pipelining scheme.

In some embodiments of the invention, analog paths 209 (Fig. 2) of analog line cards 104 operate at the same predetermined rate at which data is fed to digital processing card 108. Alternatively, analog paths 209 operate at lower rates and switch card 106 provides digital processing card 108 with consecutive data segments which are directed to different line cards 104, such that analog paths 209 will have finished handling previously received data when an additional data segment is received.

In some embodiments of the invention, switch card 106 provides digital processing card 108 with data segments of each handled connection, sequentially according to a predetermined order. Alternatively or additionally, the data segments are fed according to the quality of service (QoS) of the connections and/or the load of data in the transmission buffers of the connections.

In some embodiments of the invention, the data segments transmitted from switch card 106 to digital processing card 108 include a header which identifies the connection to which the data segment belongs. Optionally, input bus interface 302 removes the header from the data segment before the segment is forwarded to transmission path 300. The header and/or data from the header is optionally forwarded to output bus interface 332 to be used in

generating a header for the processed data segment, which is transmitted to its respective line card 104. Optionally, bus interface 332 matches the headers it receives with the respective processed data according to the processing time required by transmission path 300.

In some embodiments of the invention, input bus interface 352 receives data segments from analog line cards 104 at a predetermined rate. The received data segments are then passed through reception path 350. The processed data segments are passed by output bus interface 354, optionally at the same predetermined rate, to switch card 106, over bus 112. In some embodiments of the invention, data segments received by input bus interface 352 include a header which identifies the connection of the data segment. Input bus interface 352 optionally removes the header and passes its contents to output bus interface 354 which reinstalls the header after the data segment was processed by reception path 350.

In some embodiments of the invention, each of line cards 104 has an internal clock which sets its transmission times of received data segments to digital card 108 such that the data segments do not collide with other received data segments transmitted from other line cards 104. Alternatively or additionally, switch card 106 controls the transmission of signals from line cards 104 to digital card 108, for example by transmitting timing signals to each of line cards 104 when it is their turn to transmit a data segment to digital card 108. Further alternatively or additionally, each of line cards 104 has a separate bus portion on which it transmits the data segments it receives to digital card 108. The separate bus portions may be physically separate bus portions and/or may operate at different frequencies and/or with different codes.

Fig. 4 is a schematic block diagram showing the hardware modules of digital processing card 108, in accordance with an embodiment of the present invention. In some embodiments of the invention, digital card 108 comprises one or more pre-Fourier chips 340, one or more Fourier chips 342 and one or more reception chips 344. In some embodiments of the invention, digital card 108 further comprises one or more external memory units 346 which operate as interleaver memory 324 and/or as mapper memory 319. Optionally, each pre-Fourier chip 340 has an associated memory chip 346. Alternatively, one or more of pre-Fourier chips 340 is associated with a plurality of memory chips 346 and/or one or more of memory chips 346 is used by a plurality of pre-Fourier chips 340. External memory units 346 may comprise substantially any suitable memory units, for example SDRAM memory units. Alternatively or additionally to using external memory units 346, pre-Fourier units 340

include internal memory units. Optionally, reception chips 344 include internal memory units. Alternatively or additionally, digital card 108 includes one or more external memory units for reception chips 344.

Optionally, the number of chips of each type (340, 342 and 344) included in card 108 are chosen such that the chips of each type can handle together, at least the number of ADSL connections which can be handled by all of the analog paths 209 (Fig. 2) of all the analog line cards 104 which fit into rack 102. In some embodiments of the invention, all of chips 340 can handle the same number of ADSL connections as all of chips 342 and/or chips 344. In an exemplary embodiment of the invention, digital processing card 108 comprises three pre-Fourier chips 340, five Fourier chips 342 and two (or three) reception chips 344. In an exemplary embodiment of the invention, rack 102 holds up to thirteen line cards 104, each line card 104 handling between about 70-80 ADSL connections. Accordingly, each of chips 340 can handle at least about 320-350 ADSL connections. The handling of a plurality of ADSL connections by a single chip 340 is possible due to the speed at which chip 340 handles data. It will therefore be understood by those skilled in the art that with the advance of technology, the number of connections handled by a single chip will increase.

In some embodiments of the invention, pre-Fourier chip 340 comprises CRC unit 306, scrambler 308, FEC 310, interleaver 312, framer 314, tone ordering unit 316 and mapper 318. Fourier chip 342 optionally comprises inverse Fourier unit 326, as inverse Fourier unit 326 is relatively large. Reception chip 344 optionally comprises all the units of reception path 350, as in ADSL reception path 350 handles much less data than transmission path 300. Optionally, shifter 328 and IIR filter 330 are also included in reception chip 344, so as not to require an additional chip. Alternatively, shifter 328 and IIR filter 330 are included in chips 340 or 342 or are located on a separate chip. Further alternatively, any other division of the units of digital card 108 between chips is used. Optionally, the division is performed in a manner which minimizes the number of chips required on digital card 108.

In some embodiments of the invention, chips 340, 342 and/or 344 comprise one or more dedicated ASICs. Alternatively or additionally, one or more of chips 340, 342 and/or 344 comprise one or more processors, for example, a digital signal processor (DSP), a programmable media processor and/or a general purpose processor.

Alternatively or additionally to inverse Fourier unit 326 including an electronic processing unit, inverse Fourier unit 326 comprises an optical processing unit which performs

the inverse Fourier transform. Inverse Fourier unit 326 may be, for example, as described in Israel patent application 141,856, filed March 7, 2001, or in Israel patent application 135,576, filed April 10, 2000, the disclosures of which documents are incorporated herein by reference. In some embodiments of the invention, inverse Fourier unit 326 is partially electronic and partially optical, for example as described in PCT publication WO00/72108, the disclosure of which is incorporated herein by reference. For example, inverse Fourier unit 326 may include an optical unit which performs the Fourier transform for some of the ADSL connections and an electrical unit which performs the Fourier transform for the remaining ADSL connections. Optionally, when digital card 108 includes an optical processing unit, the card may be thicker than line cards 108, for example about 1.5 times thicker, in order to fit the optical apparatus. Rack 102 may, in such cases, carry fewer cards 104.

It is noted that by using a synchronous path from analog paths 209 to switch card 106, there is no need to manage buffers on digital card 108 and/or on analog line cards 104. Therefore, more of the space of the cards 104 and 108 may be used for processing circuitry. Alternatively to operating a synchronous path between analog paths 209 and switch card 106, buffers are used at one or more points in the signal path, in order to relax the timing constraints on digital card 108 and/or on backplane bus 112. Optionally, each connection has a separate buffer. Alternatively or additionally, a common buffer is used for some or all of the connections. The buffers may be located, for example, in bus interfaces 302, 332, 352 and/or 354.

Fig. 5 is a schematic illustration of a distributed DSLAM 500, in accordance with an alternative embodiment of the present invention. Distributed DSLAM 500 comprises a central unit 502 which includes a rack 102 which carries one or more digital cards 108 and one or more switch cards 106. Rack 102 also carries one or more remote cards 510 which connect to one or more remote units 512. Remote unit 512 optionally carries one or more analog line cards 104 which connect cable wire pairs 110 to client ADSL modems 516. It is noted that the line cards of remote unit 512 may take on substantially any shape and/or casing known in the art, and are not limited to a card shape which fits into a rack. Using remote unit 512, the same digital card 108 can service client ADSL modems 516 distanced from each other and/or from digital card 108 by tens or even hundreds of kilometers. Thus, the cost of providing ADSL service is reduced. Furthermore, remote unit 512, which needs to be located within a few kilometers from client modem 516, includes substantially only simple analog units which

generally have much lower maintenance requirements than digital card 108. Therefore, digital cards 108 may be positioned at a location which is highly accessible to maintenance personal even though the location is beyond the ADSL service range from client modems 516 serviced by the digital cards. Also, a single digital card 108 and/or a single rack 102 may service a plurality of analog cards which are distanced from each other.

Remote unit 512 optionally connects to remote card 510 through an optical fiber 514. Alternatively or additionally, any other digital link is used to transmit signals between remote unit 512 and remote card 510. In some embodiments of the invention, rack 102 additionally carries one or more line cards 104 which connect directly (e.g., through respective line interfaces 111), to one or more copper wire pairs 110.

In operation, signals transmitted to a client modem 516 serviced by a remote unit 512 are passed, after their digital processing, from digital card 108 to remote card 510. Remote card 510 transmits the signals to the respective remote unit 512 which performs analog processing on the signals and transmits the analog signals to the client modem 516. Signals from the client modem 516 are transmitted to remote unit 512 which performs analog processing which converts the signals into digital signals. The digital signals are transmitted to remote card 510 which forwards the signals to digital card 108. Remote card 510 optionally comprises one or more buffers which regulate the flow of signals to and/or from remote unit 512.

Although in the above description the tasks of a DSLAM were described as being divided between an analog card 104 and a digital card 108, in some embodiments of the invention, other divisions of the tasks are used. For example, in some embodiments of the invention, line cards 104 include one or more of the digital units, such as CRC unit 306 and scrambler 308. Such a division allows more room on digital card 108 for the heavy tasks of inverse Fourier unit 326. Alternatively or additionally, reception path 350 is located on line cards 104 instead of being on digital card 108. In some embodiments of the invention, the tasks of the DSLAM for a single connection are divided between more than two cards. For example, a first card may perform the analog tasks, a second card performs the tasks of Pre-Fourier chip 340 and a third card performs the remaining tasks. Alternatively or additionally, the units of digital card 108 are distributed between two cards, for example due to lack of space on a single card. For example, transmission path 300 may be included on one card and reception path 350 on another card. Optionally, in this example, data required for digital echo

cancellation is exchanged between the cards on backplane bus 112. Alternatively, analog echo cancellation is performed or echo cancellation is not performed. Alternatively or additionally, transmission path 300 for some connections is located on a first card while transmission path 300 for the remaining connections is located on a second card.

Furthermore, in some embodiments of the invention, a single card performs the tasks of switch card 106 and of digital card 108. Alternatively or additionally, some of the tasks of switch card 106 are transferred to digital card 108 and/or some of the tasks described above as being performed by digital card 108 are performed by switch card 106.

Although the above description relates to ADSL DSLAMs, the principles of the present invention may be used also in implementing VDSL DSLAMs.

It will be appreciated that the above described methods may be varied in many ways, including, changing the order of steps, and/or performing a plurality of steps concurrently. It should also be appreciated that the above described description of methods and apparatus are to be interpreted as including apparatus for carrying out the methods, and methods of using the apparatus. The present invention has been described using non-limiting detailed descriptions of embodiments thereof that are provided by way of example and are not intended to limit the scope of the invention. It should be understood that features and/or steps described with respect to one embodiment may be used with other embodiments and that not all embodiments of the invention have all of the features and/or steps shown in a particular figure or described with respect to one of the embodiments. Variations of embodiments described will occur to persons of the art. Furthermore, the terms "comprise," "include," "have" and their conjugates, shall mean, when used in the claims, "including but not necessarily limited to."

It is noted that some of the above described embodiments may describe the best mode contemplated by the inventors and therefore may include structure, acts or details of structures and acts that may not be essential to the invention and which are described as examples. Structure and acts described herein are replaceable by equivalents which perform the same function, even if the structure or acts are different, as known in the art. Therefore, the scope of the invention is limited only by the elements and limitations as used in the claims.

CLAIMS

1. A method of handling an ADSL connection by an access multiplexer, comprising:

receiving a data segment to be transmitted by the access multiplexer;

performing digital processing of the data segment by a digital card;

locally transferring the digitally processed data segment to a line card separate from the digital card;

performing at least analog processing of the data segment by the line card; and

transmitting the analog processed data segment on the ADSL connection.

2. A method according to claim 1, wherein performing the digital processing by the digital card comprises performing a Fourier transform.

3. A method according to claim 1 or 2, wherein performing the digital processing by the digital card comprises performing substantially all the digital processing tasks required for transmission of ADSL data.

4. A method according to claim 1 or 2, wherein performing the digital processing by the digital card comprises performing fewer than all the digital processing tasks required for transmission of ADSL data.

5. A method according to any of the preceding claims, wherein the line card performs substantially only analog tasks.

6. A method according to any of the preceding claims, wherein the line card performs at least one digital ADSL task.

7. A method according to any of the preceding claims, wherein transferring the digitally processed data to the line card comprises transferring over a backplane bus of a rack hosting both the line card and the digital card.

8. A method according to any of claims 1-6, wherein transferring the digitally processed data to the line card comprises transferring to a different rack in a same locale.

9. A method according to any of the preceding claims, wherein transferring the digitally processed data to the line card comprises transferring through an optical fiber.

10. A method of transmitting data on a plurality of ADSL connections, by an access multiplexer, comprising:

receiving a plurality of data segments, to be transmitted on a plurality of different ADSL connections, by the access multiplexer;

performing digital processing of the data segments by a digital card;

locally transferring at least one of the digitally processed data segments to a first line card and at least one of the digitally processed data segments to a second line card, separate from the first line card;

performing, by the first and second line cards, at least analog processing of the data segments transferred to the line cards; and

transmitting the analog processed data segment on their respective ADSL connections.

11. A method according to claim 10, wherein the first and second line cards are not positioned in a common rack.

12. A method according to claim 10, wherein the first and second line cards are positioned in a common rack.

13. A method of handling an ADSL connection by an access multiplexer, comprising:

receiving an analog data segment from the ADSL connection, by a line card;

performing at least analog processing of the data segment by the line card;

locally transferring the analog processed data segment to a digital card separate from the analog card; and

performing at least one ADSL digital processing task of the data segment by the digital card.

14. A method according to claim 13, wherein performing the digital processing by the digital card comprises performing substantially all the digital processing tasks required for reception of ADSL data.

15. A method according to claim 13, wherein performing the digital processing by the digital card comprises performing fewer than all the digital processing tasks required for reception of ADSL data.

16. A DSL access multiplexer, comprising:

at least one line card including one or more analog units adapted to transmit signals on one or more respective ADSL connections;

a digital processing card adapted to perform at least one digital ADSL handling task on signals to be transmitted; and

a local communication link adapted to transfer signals processed by the digital processing card to one of the at least one line cards.

17. A multiplexer according to claim 16, wherein the at least one line card includes substantially only analog units.

18. A multiplexer according to claim 16 or 17, wherein the at least one digital processing card includes a Fourier transform unit.

19. A multiplexer according to any of claims 16-18, wherein the communication link comprises a backplane of a rack adapted to receive the at least one line card and the digital processing card.

20. A multiplexer according to any of claims 16-19, wherein the communication link comprises an optical fiber.

21. A DSL access multiplexer, comprising:

at least 64 analog units adapted to transmit signals on one or more respective ADSL connections; and

a single digital processing unit adapted to perform at least one digital ADSL handling task on signals to be transmitted by all the at least 64 analog units.

22. A multiplexer according to claim 21, wherein the at least 64 analog units are included in a plurality of line cards.

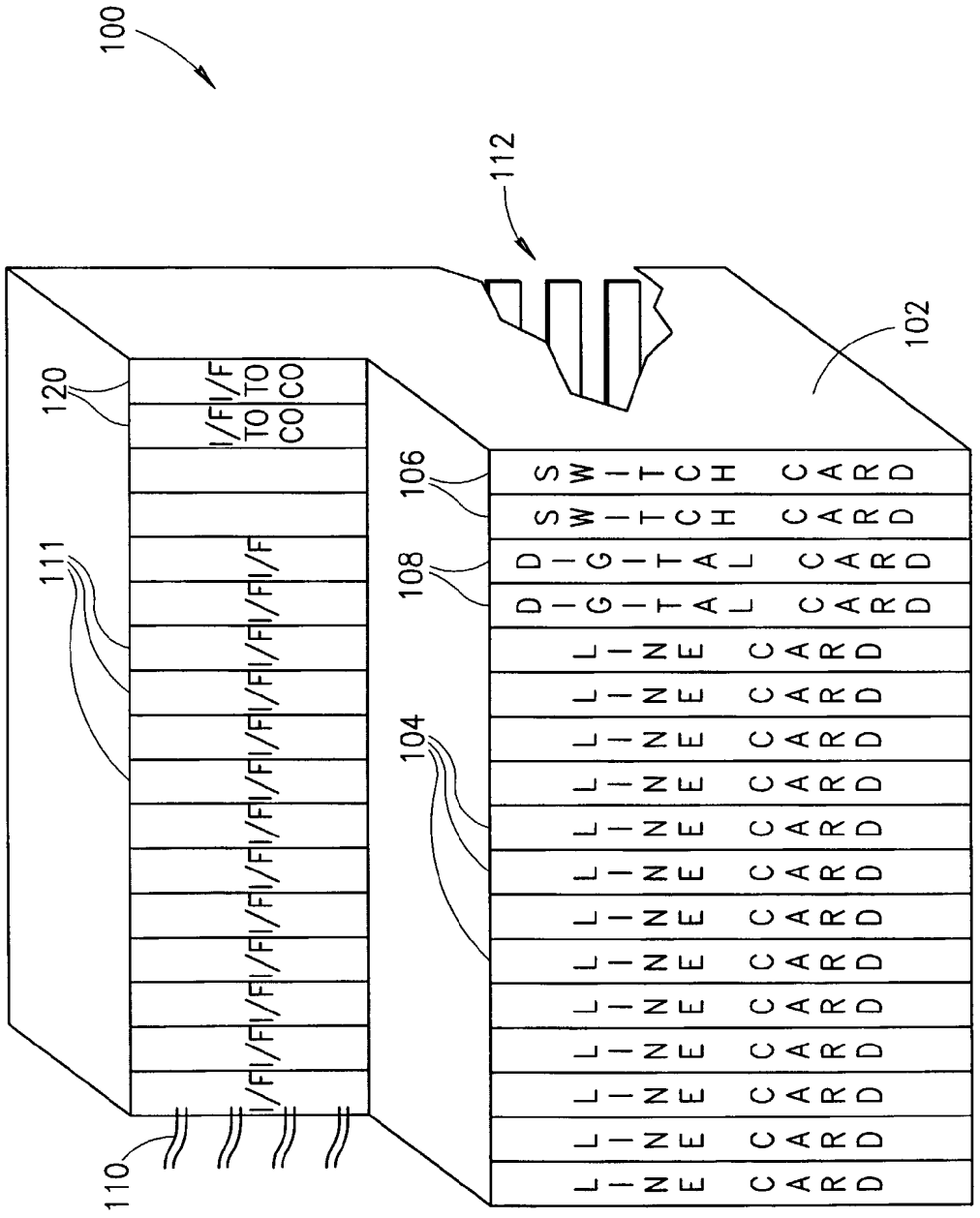

100
112
102
120
111
106
108
104
110
I/FI/F TO CO
LINE CARD
DIGITAL SWITCH
DIGITAL LINE CARD
LINE CARD

FIG.1

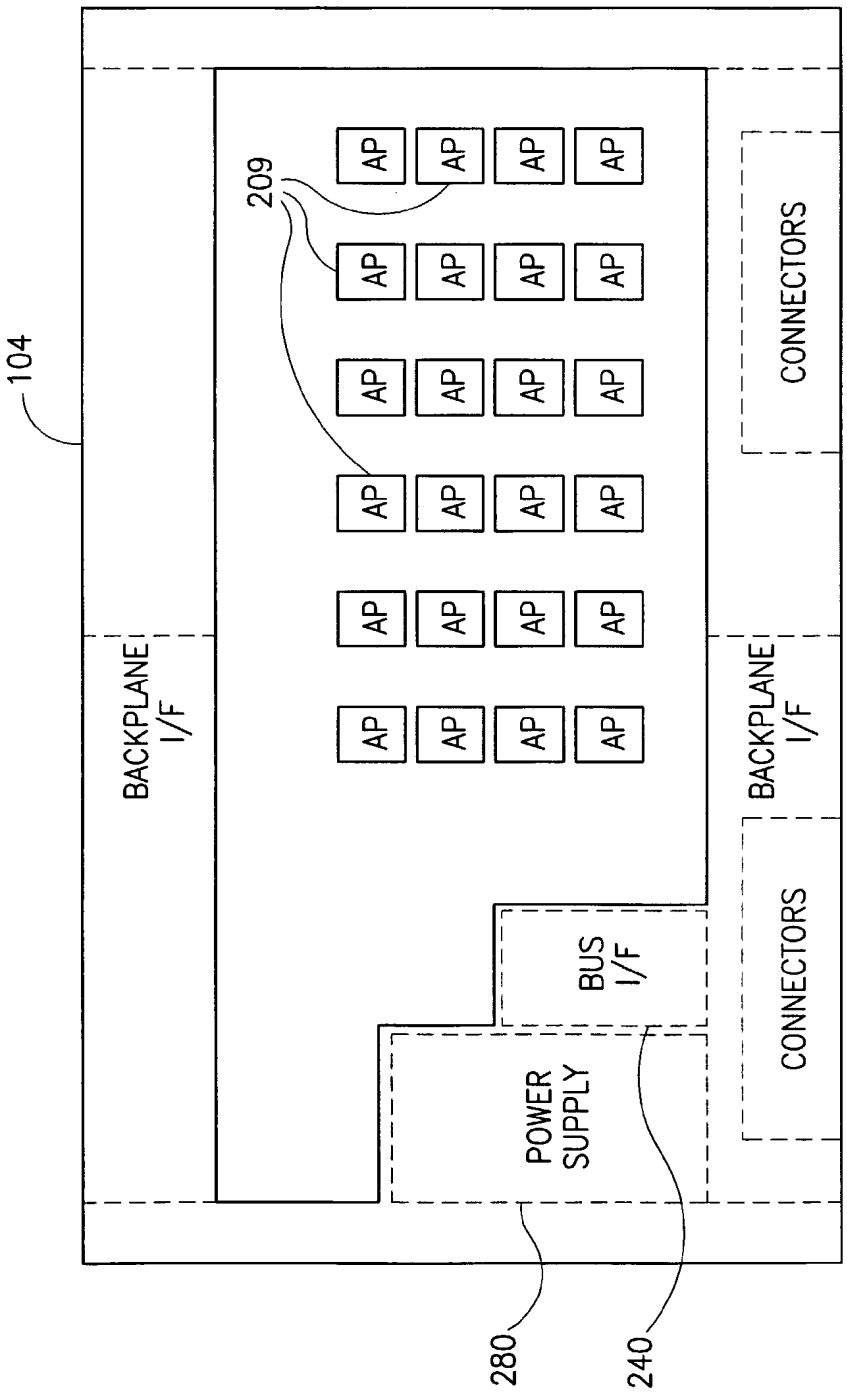
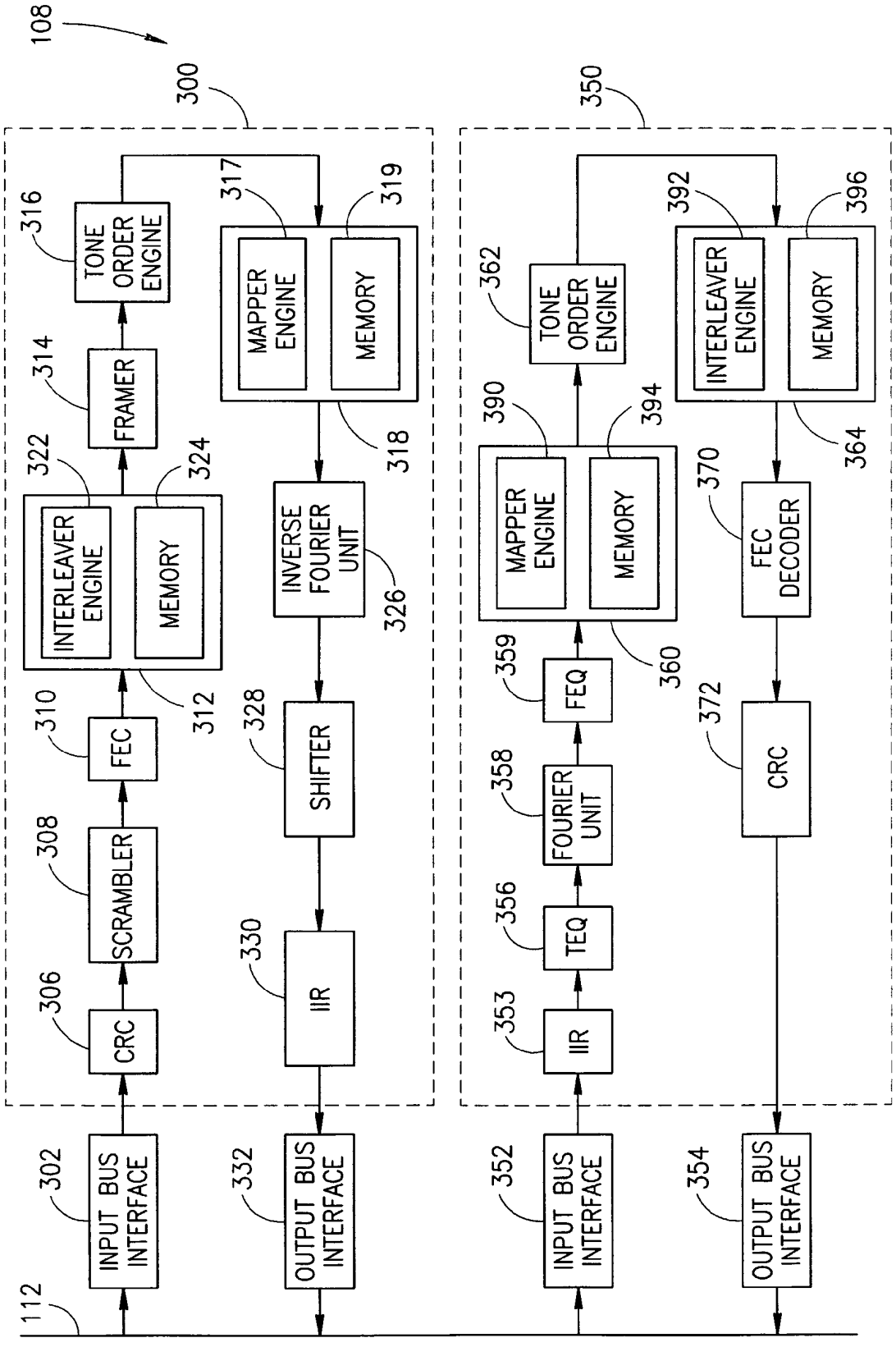

104
209
AP
BACKPLANE I/F
CONNECTORS
BUS I/F
POWER SUPPLY
280
240

FIG.2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300
350
112
INPUT BUS INTERFACE
302
CRC
306
SCRAMBLER
308
FEC
310
INTERLEAVER ENGINE
322
MEMORY
324
312
FRAMER
314
TONE ORDER ENGINE
316
MAPPER ENGINE
317
MEMORY
319
318
INVERSE FOURIER UNIT
326
SHIFTER
328
IIR
330
OUTPUT BUS INTERFACE
332
INPUT BUS INTERFACE
352
IIR
353
TEQ
356
FOURIER UNIT
358
FEQ
359
MAPPER ENGINE
390
MEMORY
394
360
TONE ORDER ENGINE
362
INTERLEAVER ENGINE
392
MEMORY
396
364
FEC DECODER
370
CRC
372
OUTPUT BUS INTERFACE
354

FIG.3

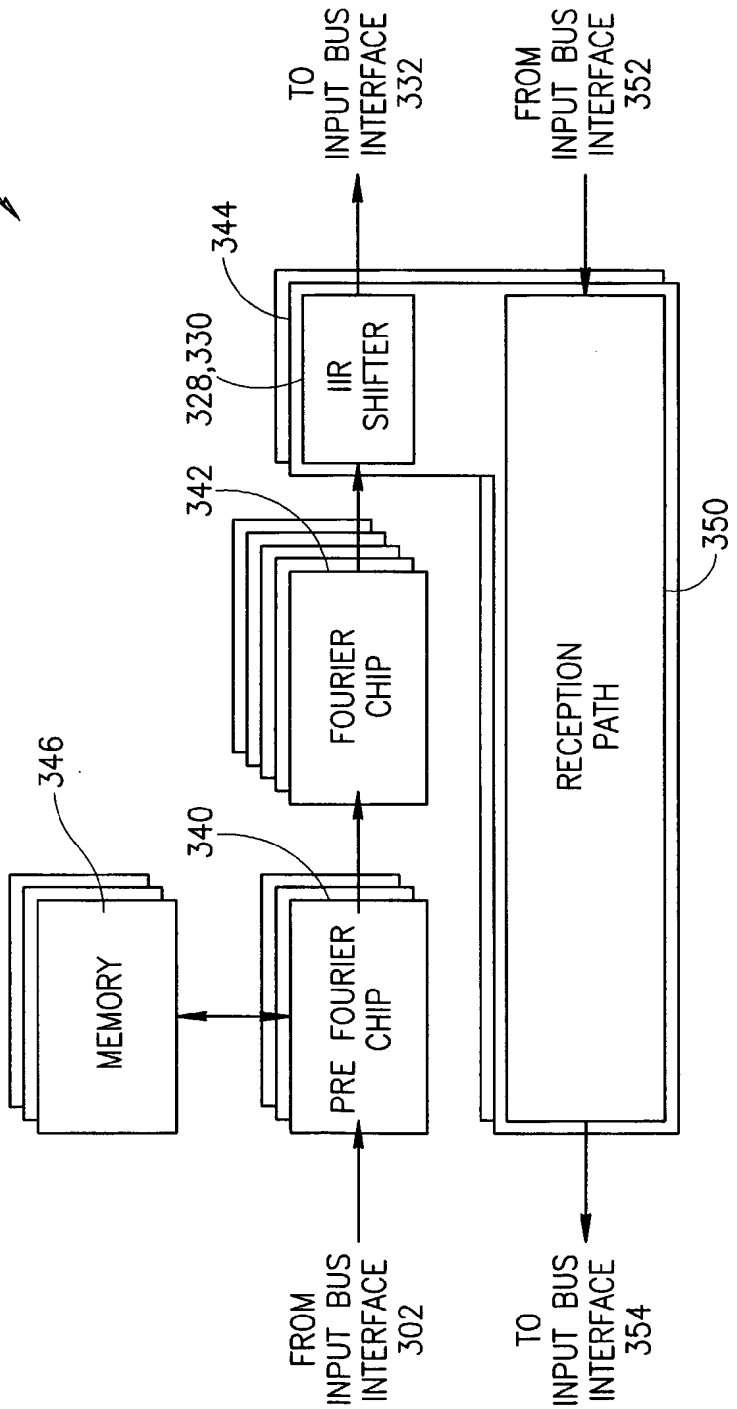
108
TO INPUT BUS INTERFACE 332
FROM INPUT BUS INTERFACE 352
344
328,330
IIR SHIFTER
342
FOURIER CHIP
350
RECEPTION PATH
346
340
MEMORY
PRE FOURIER CHIP
FROM INPUT BUS INTERFACE 302
TO INPUT BUS INTERFACE 354

FIG.4

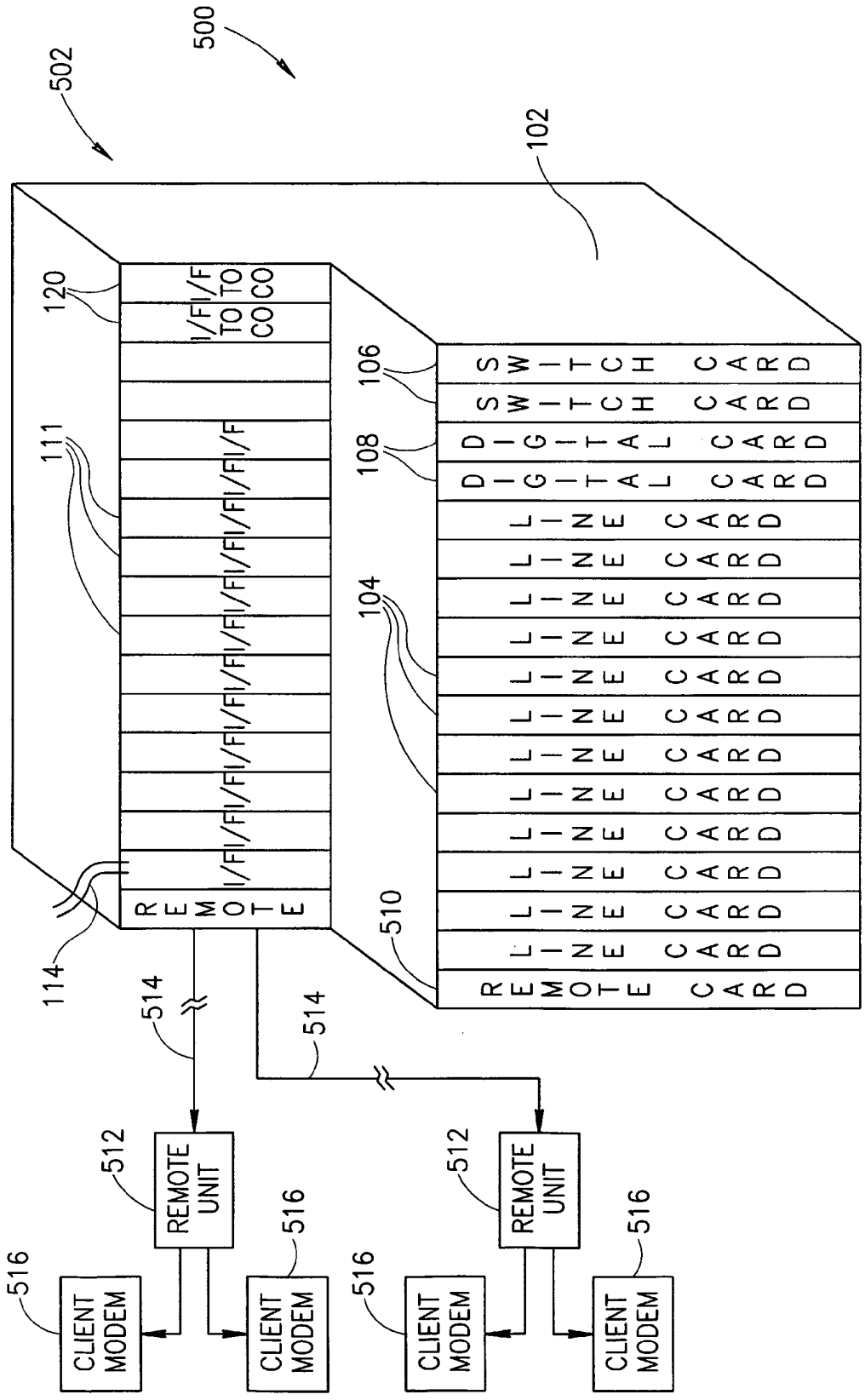
500
502
102
120
106
108
111
104
510
114
514
514
512
512
REMOTE UNIT
REMOTE UNIT
516
516
516
516
CLIENT MODEM
CLIENT MODEM
CLIENT MODEM
CLIENT MODEM

FIG.5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IL02/00273

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H04L 12/26
US CL : 370/252,419;375/260;725/103

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 370/252,419;375/260;725/103

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,594,491 A (HODGE et al) 14 January 1997 (14.01.1997), column 1, lines 59-61, column 2, lines 59-60, column 3, lines 57-60, column 4, lines 24-25 and lines32.	1-22
Y	US 6,137,839 A (MANNERING et al) 24 October 2000 (24. 10. 2000), column 1, lines 66-67, column 2, line 53, column 2, lines 59-60, column 4, line 32 , lines 43-44, column 8, lines 1-2, column 9, lines 40-41 and lines 45-53, column column 13, lines 41-42,	1-22

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 July 2002 (20.07.2002)	22 AUG 2002
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No.	Authorized officer Inder Mehra Telephone No. 703-304-4700

Form PCT/ISA/210 (second sheet) (July 1998)